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EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/714,246	DI BENEDETTO ET AL.	
	Examiner	Art Unit	
	Ian N. Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4,6-13 and 15-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-4,6-11,16,17,19,20,22,23,25,26,28 and 29* is/are allowed.

6)☒ Claim(s) *12,13,15,18,21,24 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9-7-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kicklighter (U.S. 6,005,841) in view of Freedman (U.S. 4,342,083).

Regarding Claim 12, Kicklighter discloses an intermediate network device for use in a computer network (see FIG. 1, a network switch 2), the network device comprising:

a first supervisor card (see FIG. 1, PRI 38(A)) in communicating relationship (see FIG. 1, Switching Buses 30) with the one or more line cards (see FIG. 1, Line Cards IO 20);

a second supervisor card (see FIG. 1, PRI 38(S) in communication relations (see FIG. 1, Switching Buses 30) with the first supervisor card;

an application loaded onto the first and second supervisor cards (see col.5, lines 65 to col.6, lines 18), the application configured to define and manipulate a plurality of state variables (see col. 4, lines 51-55; the configuration/switching/synchronizing/ management/supervisory application defines/performs/runs/executes/manipulates the plurality of events/tasks/states occurrences (i.e. state variables)); and

at least one line card (see FIG. 1, Line Cards IO 20) defining a plurality of ports for forwarding messages (see FIG. 1, Line Cards IO receives and transmits the frames) across the computer network (see col. 2, lines 5-7), the at least one line card in communicating relationship

with the first and second supervisor cards and configured to receive and state information from the application (see FIG. 1, Line cards communicate with PRI 38(A) and PRI (B) via buses and via Nodal Switch or CPU/matrix 44);

a high availability entity (see FIG. 2, PRI 38 and 30a-b) disposed on the first and second supervisor cards, the high availability entities comprising:

an event mechanism (see FIG. 2, components 30a, 30b, 60,62,64,66,68,70,72,74,76, 78,80,84,86 and 88) for notifying a selected one of the first or second supervisor cards of changes to the application's state variables (see col. 2, lines 24-34); and

a database mechanism (see FIG. 2, ROM 90, RAM 92, shared RAM 82) for storing the state variables at the first and second supervisor cards (see col. 2, lines 34-39).

the state variables stored at the first and second supervisor cards are consistent with the port state information maintained at the at least one line card (see FIG. 2; PRI 38 card commands/instructs the line card IO (via Nodal Switch or CPU/matrix 44) to update/change the switching/ management/supervisory events/tasks/conditions/states; see col. 4, lines 51-67. Each line card is the IO (Input and output) module, and it must have a memory/caching mechanism to maintain/store the command/instruction of the state information of each port. Thus, it is clear that plurality of events/tasks/states occurrences (i.e. state variables) in both PRI 38 cards are consistent with each line card's call processing or framing states/tasks information (i.e. port states).)

Kicklighter does not explicitly disclose a sequence mechanism resetting the line card/system in the event that the state variable and the port state information differ after a failure of one of the first or second cards/systems. However, it is well known in the art that when a

command/instruction is generated by the processor/controller, it must have a sequence number, timer, time-stamp, or clock cycle that identifies a particular instruction/command along with the contents of the instruction/command so that the recipient can identify, store, and performs tasks synchronously. Freedman discloses a sequence mechanism for ensuring the state variables (see FIG. 4, sampling number; see col. 13, lines 36-55) stored (see FIG. 3, Memory 16; see col. 7, lines 60-65) at the first and second systems (see FIG. 2, Application computers 100n) are consistent with state information (see FIG. 4, tasks information) maintained at the at the line system (see FIG. 2, Application computer 100a-b; see col. 15, lines 60), and resetting the at least one line card/system (see FIG. 5, Synchronizer 226; see col. 16, lines 34-52) in the event that the state variable and the state information differ (see col. 15, lines 52-60) after a failure of one of the first or second cards/system (see col. 16, lines 11-21).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide synchronization mechanism between different systems after failure of one system, as taught by Freedman in the system of Kicklighter, so that it would permit each computer system to communicate with every other computer in the system to coordinate the execution tasks; see Freedman col. 2, line 10-45, and it would ensure more reliable increase the recipient capability to identify, store, and performs commanded/instructed tasks synchronously.

Regarding Claim 13, Kicklighter discloses the first supervisor card is designated as an active supervisor card (see FIG. 1, PRI 38(A) as active) and the second supervisor card is designated as a standby supervisor card (see FIG. 1, PRI 38(S) as standby) for the network device; see col. 6, lines 35-36;

the application is allowed to run on the active supervisor card but not on the standby supervisor card (see col. 2, lines 13-20; note the PRI 38(S) is placed in a standby/listening mode, thus, it does not execute any task/applications);

in response to a crash or failure of the active supervisor card, the application carries on its execution from the standby supervisor card utilizing at least some of the state variables stored at the database mechanism of the standby supervisor card (see col. 2, lines 39-44; note that when PRI 38(A) fails, the PRI 38(S) continues the servicing/performing/executing the events/tasks/applications just prior to failure according to the stored/hold events/tasks/applications.)

3. Claim 15,18,21,24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horst (5,838,894) in view of Ronstrom (U.S. 6,438,707).

Regarding Claim 15, Horst discloses method for operating a network device (see FIG. 1A, data processing system 10), comprising:

operating an active supervisor (see FIG. 1A, CPU 12A), the active supervisor receiving state information (see FIG. 23, interface unit 24a receives information symbols and its T_ClK; see col. 74, lines 55 to co. 75, lines 44) from at least one line card (see FIG. 1, Router 14A or B or system 10);

generating a sequence (see FIG. 31B, SYNC CLK; see col. 76, lines 40-46) by the active supervisor in response to receipt of state information (see col. 75, lines 60 to col. 76, lines 16, 41-46; also see FIG. 33A, step 1050);

returning the sequence to the at least one line card (see FIG. 31A, step 956, sending SYNC CLK; see col. 77, lines 25-35; also see FIG. 33A, step 1052-1053);

storing the state information and sequence to a standby supervisor (see FIG. 1, CPU 10B; see FIG. 25, a signal line 667 from CPU 10A to Clock generator 654B for SYNC CLK; see col. 66, lines 44 to col.67; see col. 67, lines 12-45; see FIG. 33B, step 1080,1082,1084)

in response to a failure of the active supervisor, switching control to the standby supervisor (see FIG. 32, step 1012; see col. 78, lines 45-60; see col. 80, lines 36-64);

comparing, by the standby supervisor, a stored sequence with a reported sequence, the reported sequence number reported by a line card (see col. 77, lines 21 to col. 78, lines 40; note that CPU clock SYN_CLK and router clock must be compared before resting the clock); and

resetting the line card in the event that the reported sequence number is different than the stored sequence number (see FIG. 31A, step 960, router clock reset; see col. 77, lines 38-60; see col. 78, lines 64 to col. 79, lines 15).

Horst does not explicitly disclose sequence number. It is well known in the art the when a working CPU fails, the standby process must take over the processing which involves resynchronization the processing sequence numbers and events between all components within the system. Ronstrom teaches operating an active supervisor (see FIG. 1, Primary System PS 100), the active supervisor receiving state information (see FIG. 1, communication means 130; see col. 7, lines 1-40; see FIG. 6, step 601, event message; see col. 16, lines 55-65); generating a sequence number (see FIG. 6, process sequence number A, B(1),C,B(2), or D) by the active supervisor in response to receipt of the state information (see FIG. 1, Event Generator EG 103; see col. 7, lines 56 to col. 8, lines 6; see col. 5, lines 50-60); storing the state information and

sequence number to a standby supervisor (see FIG. Primary Memory PM 102; see col. 7, lines 6-19); comparing, by the standby supervisor, a stored sequence number with a reported sequence number (see FIG. 5, step 507, 509; see col. 16, lines 5-20); resetting in the event that the reported sequence number is different than the stored sequence number (see FIG. 5, step 510, recovery process; see col. 16, lines 18-25; see FIG. 7, 701-711; see col. 18, lines 25 to col. 19, lines 10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide sequencing the event utilizing a sequence number and synchronizing by utilizing the sequence number after a failure as part of the recovering process, as taught by Ronstrom in the system of Horst, so that it would provide a fault tolerant system requiring a low communication load between systems while allowing high level of synchronization; see Ronstrom col. 1, line 44-55.

Regarding Claim 18, Horst discloses a network device (see FIG. 1A, data processing system 10), comprising:

at least one line card (see FIG. 1, Router 14A or B or system 10);

an active supervisor (see FIG. 1A, CPU 12A), the active supervisor to receive state information from at least one line card (see FIG. 23, interface unit 24a receives information symbols and its T_ClK; see col. 74 , lines 55 to co. 75, lines 44), generate a sequence (see FIG. 31B, SYNC CLK; see col. 76, lines 40-46) in response to receipt of the state information (see col. 75, lines 60 to col. 76, lines 16, 41-46; also see FIG. 33A, step 1050), and return the sequence number to the at least one line card (see FIG. 31A, step 956, sending SYNC CLK; see col. 77, lines 25-35; also see FIG. 33A, step 1052-1053); a standby supervisor, the standby supervisor to store the state information and sequence (see FIG. 1, CPU 10B; see FIG. 25, a

signal line 667 from CPU 10A to Clock generator 654B for SYNC CLK; see col. 66, lines 44 to col.67; see col. 67, lines 12-45; see FIG. 33B, step 1080,1082,1084), wherein if the active supervisor fails and control is switched to the standby supervisor (see FIG. 32, step 1012; see col. 78, lines 45-60; see col. 80, lines 36-64), the standby supervisor is to compare a stored sequence with a reported sequence, the reported sequence reported by a line card (see col. 77, lines 21 to col. 78, lines 40; note that CPU clock SYN_CLK and router clock must be compared before resting the clock), and to reset the line card if the reported sequence number is different than the stored sequence (see FIG. 31A, step 960, router clock reset; see col. 77, lines 38-60; see col. 78, lines 64 to col. 79, lines 15).

Horst does not explicitly disclose sequence number. It is well known in the art the when a working CPU fails, the standby process must take over the processing which involves resynchronization the processing sequence numbers and events between all components within the system. Ronstrom teaches operating an active supervisor (see FIG. 1, Primary System PS 100), the active supervisor receiving state information (see FIG. 1, communication means 130; see col. 7, lines 1-40; see FIG. 6, step 601, event message; see col. 16, lines 55-65); generating a sequence number (see FIG. 6, process sequence number A, B(1),C,B(2), or D) by the active supervisor in response to receipt of the state information (see FIG. 1, Event Generator EG 103; see col. 7, lines 56 to col. 8, lines 6; see col. 5, lines 50-60); storing the state information and sequence number to a standby supervisor (see FIG. Primary Memory PM 102; see col. 7, lines 6-19); comparing, by the standby supervisor, a stored sequence number with a reported sequence number (see FIG. 5, step 507, 509; see col. 16, lines 5-20); resetting in the event that the reported sequence number is different than the stored sequence number (see FIG. 5, step 510, recovery

process; see col. 16, lines 18-25; see FIG. 7, 701-711; see col. 18, lines 25 to col. 19, lines 10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide sequencing the event utilizing a sequence number and synchronizing by utilizing the sequence number after a failure as part of the recovering process, as taught by Ronstrom in the system of Horst, so that it would provide a fault tolerant system requiring a low communication load between systems while allowing high level of synchronization; see Ronstrom col. 1, line 44-55.

Regarding Claim 21, the device claim, which has substantially disclosed all the limitations of the respective device claim 18 and method claim 15. Therefore, it is subjected to the same rejection.

Regarding Claim 24, the computer readable medium processing the method claim, which has substantially disclosed all the limitations of the respective device claim 18 and method claim 15. Therefore, it is subjected to the same rejection.

Regarding Claim 27, the electromagnetic signals on a processor for the practice of the method claim, which has substantially disclosed all the limitations of the respective device claim 18 and method claim 15. Therefore, it is subjected to the same rejection.

Response to Arguments

4. Applicant's arguments, see page 17-19, filed 9/2/05, with respect to Claim 16,17,19,20,22,23,25,26,28 and 29 have been fully considered and are persuasive. The rejection of claims 16,17,19,20,22,23,25,26,28 and 29 have been withdrawn.

5. Applicant's arguments filed 2-22-2005, regarding claims 12,13, 15,18,21,24,27 have been fully considered but they are not persuasive.

Regarding claim 12, the applicant argued that, "...the combination of Kicklighter and Freedman are silent...a sequence mechanism for ensuring the state variables stored at the first and second supervisor cards are consistent with the port state information maintained at the at least one line card, the sequence mechanism and resetting the at least one line card/system in the event that the state variable and the state information differ after a failure of one of the first or second supervisor cards..." in page 22, paragraph 2 and 5.

In response to applicant's argument, the examiner respectfully disagrees with the argument above. In particular, Kicklighter teaches the state variables stored at the first and second supervisor cards are consistent with the port state information maintained at the at least one line card (see FIG. 2; PRI 38 card commands/instructs the line card IO (via Nodal Switch or CPU/matrix 44) to update/change the switching/ management/supervisory events/tasks/conditions/states; see col. 4, lines 51-67. Each line card is the IO (Input and output) module, and it must have a memory/caching mechanism to maintain/store the command/instruction of the state information of each port. Thus, it is clear that plurality of events/tasks/states occurrences (i.e. state variables) in both PRI 38 cards are consistent with each line card's call processing or framing states/tasks information (i.e. port states).) Freedman teaches a sequence mechanism for ensuring the state variables (see FIG. 4, sampling number; see col. 13, lines 36-55) stored (see FIG. 3, Memory 16; see col. 7, lines 60-65) at the first and second systems (see FIG. 2, Application computers 100n) are consistent with state information (see FIG. 4, tasks information) maintained at the at the line system (see FIG. 2, Application

computer 100a-b; see col. 15, lines 60), and resetting the at least one line card/system (see FIG. 5, Synchronizer 226; see col. 16, lines 34-52) in the event that the state variable and the state information differ (see col. 15, lines 52-60) after a failure of one of the first or second cards/system (see col. 16, lines 11-21). Thus, the combined system of Kicklighter and Freedman discloses the argued limitation.

Regarding claim 12, the applicant argued that, "...Kicklighter is silent concerning a sequencing mechanism for state variable between supervisor and line cards. Kicklighter discusses synchronization between a CPU and a PRI-32 card...Freedman similarly lacks any disclosure of applicant's sequence mechanism..." in page 22, paragraph 3.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to applicant's argument, Kicklighter discloses concerning a sequencing mechanism for state variable between supervisor and line cards as set forth in above response. Kicklighter's RPI cards commands/instructs IO cards to synchronize by updating/changing the switching/ management/supervisory events/tasks/conditions/states; see col. 4, lines 51-67 in order to synchronize. Feedman discloses sequencing mechanism as set fort in above response. Thus, the combined system of Kicklighter and Freedman discloses the argued limitation.

Regarding claim 15, the applicant argued that, "...the combination of Horst and Ronstrom are silent regarding... comparing, by the standby supervisor, a stored sequence with a reported sequence, the reported sequence number reported by a line card; and resetting the line

card in the event that the reported sequence number is different than the stored sequence number..." page 24, paragraph 2,3; page 25, paragraph 1-2.

In response to applicant's argument, the examiner respectfully disagrees with the above argument. Horst discloses generating a sequence (see FIG. 31B, SYNC CLK; see col. 76, lines 40-46) by the active supervisor in response to receipt of state information (see col. 75, lines 60 to col. 76, lines 16, 41-46; also see FIG. 33A, step 1050); returning the sequence to the at least one line card (see FIG. 31A, step 956, sending SYNC CLK; see col. 77, lines 25-35; also see FIG. 33A, step 1052-1053); storing the state information and sequence to a standby supervisor (see FIG. 1, CPU 10B; see FIG. 25, a signal line 667 from CPU 10A to Clock generator 654B for SYNC CLK; see col. 66, lines 44 to col.67; see col. 67, lines 12-45; see FIG. 33B, step 1080,1082,1084); comparing, by the standby supervisor, a stored sequence with a reported sequence, the reported sequence number reported by a line card (see col. 77, lines 21 to col. 78, lines 40; note that CPU clock SYN_CLK and router clock must be compared before resting the clock; in order to detect the synchronization/sequence difference, one must compare two sequences/clocks); and resetting the line card in the event that the reported sequence number is different than the stored sequence number (see FIG. 31A, step 960, router clock reset; see col. 77, lines 38-60; see col. 78, lines 64 to col. 79, lines 15). Ronstrom teaches operating an active supervisor (see FIG. 1, Primary System PS 100), the active supervisor receiving state information (see FIG. 1, communication means 130; see col. 7, lines 1-40; see FIG. 6, step 601, event message; see col. 16, lines 55-65); generating a sequence number (see FIG. 6, process sequence number A, B (1), C, B (2), or D) by the active supervisor in response to receipt of the state information (see FIG. 1, Event Generator EG 103; see col. 7, lines 56 to col. 8, lines 6; see

col. 5, lines 50-60); storing the state information and sequence number to a standby supervisor (see FIG. Primary Memory PM 102; see col. 7, lines 6-19); comparing, by the standby supervisor, a stored sequence number with a reported sequence number (see FIG. 5, step 507, 509; see col. 16, lines 5-20; determine the event data/sequence do not agree by comparing); resetting in the event that the reported sequence number is different than the stored sequence number (see FIG. 5, step 510, recovery process; see col. 16, lines 18-25; see FIG. 7, 701-711; see col. 18, lines 25 to col. 19, lines 10). Thus, the combined system of Horst and Ronstrom discloses the argued limitations.

In view of the above, **the examiner respectfully disagrees** with applicant's argument and believes that the references as set forth in the 103 rejections are proper.

Allowable Subject Matter

6. Claims 2-4, 6-11, 16-17, 19-20,22-23, 25-26 and 28-29 are allowed.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM INM
11-23-05

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